

Implementation of Active Loads MOSFET Amplifiers in Vocational Training

Ionel BOSTAN

Department of Electronics and Computers Science
University of Pitești
Pitești, Romania
ionel.bostan@upit.ro

Abstract – In this paper is presented one electronic board with highly educational role, designed by author, which can be used in vocational training in the field of analog electronic. This board provides all necessary resources in order to study the advantages and disadvantages of NMOS common-sources amplifiers with or without active loads. Also this board can be useful in other experiment such MOSFET parameters estimation, studying current PMOS current mirrors, etc.

Keywords - educational electronic board, passive load common-source amplifier, active load common-source amplifier, current mirrors, analog electronics, MOSFET transistor, vocational training.

I. INTRODUCTION

For a long period of time vocational education and training (VET) played only a minor role in European countries because general opinion was that it offered less good jobs and even less promotion opportunities. In order to make VET more attractive, a series of European instruments was developed since Copenhagen Declaration, such as: (1) European Qualifications Framework (EQF); (2) European Credit system for Vocational Education and Training (ECVET); (3) European Qualifications Framework (EQF); (4) Europass framework. All these instruments provide a legal framework to support cooperation in quality assurance; recognition of qualifications; mobility and lifelong learning. The growing importance of VET it is recognized in various documents elaborated by European Centre for the Development of Vocational Training, [1].

To improve the quality, efficiency and attractiveness of VET, European Union establishes eleven strategic objectives for 2011-2020 in Bruges Communiqué. Among them, from my point of view, “encourage practical activities and the provision of high-quality information and guidance” [2], will have a great long-term impact.

In any field of vocational education, in order to make relevant practical activities, appropriate teaching materials are mandatory. In this direction, EU offer constant financial support for developing new educational materials and methodologies via transnational projects. A good example of cooperation of different educational entity in developing educational materials that meet the requirements of

European community is *One2One* [3]. Even so, the effort to develop new educational equipment must be a constant concern of each teacher [4].

In author opinion, for Analog Integrated Circuit subject there is a relative lack of appropriate educational boards due to the following facts: (1) all circuits must operate at very low bias currents; (2) each gain stage usually operates on active internal loads; (3) great difficulties in ensuring appropriate biasing of each gain stage; (4) multistage amplifier requires direct coupling.

The most common building blocks in analog integrated circuits are voltage amplifiers. Among them, voltage amplifiers using active loads are used in almost every analog integrated circuit due to their superior performance over standard configurations with passive loads. The main tow benefits of active load configurations are: (1) much higher gain at the much lower bias current; (2) active load is much easier to fabricate then high value resistor. On the other hand, due to the high gain, active load configurations are more difficult to bias, therefore requires additional circuits in order to ensure correct operation.

From didactical point of view, taking into account the importance of the active load configurations in microelectronics, it is very important for students to have the opportunity to make practical lab experiments, not only SPICE simulations, in order to have a better understanding of these circuits.

In this paper is presented one electronic board with highly educational role, which can be useful in vocational training in the field of analog electronics. With this board students can make practical experiments in order to understand the advantage and disadvantage of common-source (CS) amplifiers with or without active loads.

II. TYPICAL CS AMPLIFIERS TOPOLOGIES

The most common loads used for common-source amplifier are:

- passive (resistive) load;
- current-source load;
- diode-connected PMOS load;

- composite load made of MOSFET diode connected in parallel with current-source.

First type of load is used for discrete implementation and the last three are used only inside of integrate circuits. In this section are presented the main characteristics for each type of load for CS amplifier

A. Common-Source Amplifier with Passive Load

The first topology of amplifier which can be study on educational board is common-source stage with passive load connected as in Figure 1.

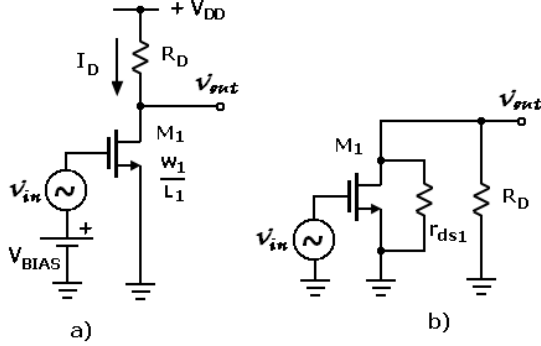


Figure 1. Common-source amplifier with passive load

For passive load CS stage, the voltage gain is estimated with relation (1)

$$a_v = -g_m R_L = -g_m (r_{ds} \parallel R_D). \quad (1)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2I_D \mu_n C_{ox} \frac{W}{L}} = \frac{I_D}{0.5 \cdot V_{OV}}. \quad (2)$$

where:

- g_m represent the transconductance of active element M1;
- V_{OV} represent the overdrive voltage of active element M1 at bias current I_D ;

In many practical situations for this type of amplifier, condition $r_{ds} \gg R_D$ is met and therefore voltage gain can be approximately calculated with relation (3)

$$a_v \cong -g_m R_D = \left(\sqrt{2I_D \mu_n C_{ox} \frac{W}{L}} \right) R_D. \quad (3)$$

For passive load CS configuration, the maximum voltage gain is obtained for no load operation [5], [6], [7], is named intrinsic gain and is given by relation (4)

$$a_{v \max} \cong \frac{V_{DD}}{0.5 \cdot V_{OV}}. \quad (4)$$

From last tow relations it can be seen that maximal voltage gain is limited by power supply voltage V_{DD} , and bias current I_D .

B. Common-Source Amplifier with Current-Source Load

The second topology which can be study on educational board is CS with active load connected as in Figure 2.

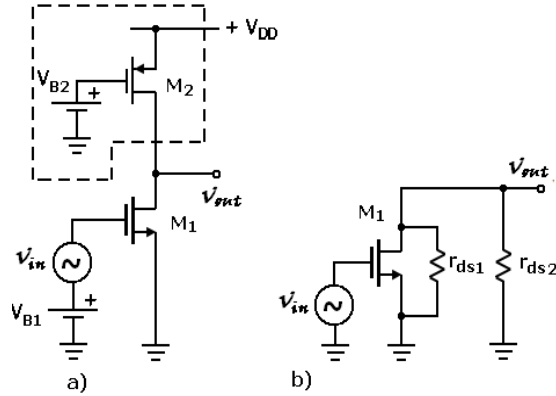


Figure 2. Common-source amplifier with active load (current source generator implemented with M_2)

For this configuration, the voltage gain is calculated using relations (5):

$$\left. \begin{aligned} a_v &= -g_{m1} R_L = -g_{m1} (r_{ds1} \parallel r_{ds2}) \\ R_L &= r_{ds1} \parallel r_{ds2} = \frac{r_{ds1} r_{ds2}}{r_{ds1} + r_{ds2}} \\ r_{ds1} &= \frac{1}{\lambda_N I_D} \\ r_{ds2} &= \frac{1}{\lambda_P I_D} \end{aligned} \right\} \Rightarrow \square$$

$$\Rightarrow a_v = -g_{m1} \frac{1}{(\lambda_N + \lambda_P) I_D}. \quad (5)$$

Furthermore, taking into the account the expressions of transconductance, voltage gain can be rewrite as:

$$\left. \begin{aligned} a_v &= -g_{m1} \frac{1}{(\lambda_N + \lambda_P) I_D} \\ g_{m1} &= \sqrt{2I_D \mu_n C_{ox} \frac{W_1}{L_1}} \end{aligned} \right\} \Rightarrow$$

$$\Rightarrow a_v = -\sqrt{2I_D \mu_n C_{ox} \frac{W_1}{L_1}} \frac{1}{(\lambda_N + \lambda_P) I_D} \quad (6)$$

$$a_v = \frac{-1}{\lambda_N + \lambda_P} \sqrt{\frac{2\mu_n C_{ox} \frac{W_1}{L_1}}{I_D}}. \quad (7)$$

In [5] it is shown that voltage gain can be expressed as a ratio between equivalent Early voltage and overdrive voltage of the active transistor M_1

$$a_v = \frac{-1}{\lambda_N + \lambda_P} \cdot \frac{1}{0.5 \cdot V_{OV1}} = -\frac{V_{Aeq}}{0.5 \cdot V_{OV1}}. \quad (8)$$

From last relation it can be seen one main advantage of this topology: voltage gain does not longer depend on supply voltage V_{DD} , therefore it can be used for low voltage supply.

C. Common-Source Amplifier with Diode – Connected PMOS Load

The third topology implemented on educational board is CS stage with diode-connected PMOS load as shown in Figure 3. This topology it is characterized by a very good linearity and has a large bandwidth.

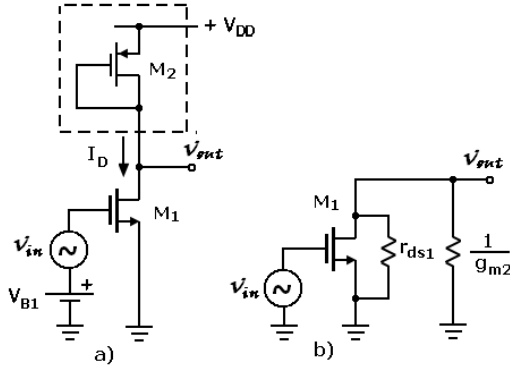


Figure 3. CS stage with diode-connected PMOS load

The drawback of this topology is given by low voltage gain [5], [6], [7].

$$a_v = -g_{m1} R_L = -g_{m1} \left(r_{ds1} \parallel \frac{1}{g_{m2}} \right) \Rightarrow \left. \begin{aligned} r_{ds1} &\gg \frac{1}{g_{m2}} \\ \Rightarrow a_v &\cong -\frac{g_{m1}}{g_{m2}} \end{aligned} \right\}. \quad (9)$$

Voltage gain relation (9) can be rewritten as:

$$\left. \begin{aligned} a_v &\cong -\frac{g_{m1}}{g_{m2}} \\ g_{m1} &= \sqrt{2I_{D1}\mu_n C_{ox} \frac{W_1}{L_1}} \\ g_{m2} &= \sqrt{2I_{D2}\mu_p C_{ox} \frac{W_2}{L_2}} \end{aligned} \right\} \Rightarrow \left. \begin{aligned} \Rightarrow a_v &\cong -\frac{\sqrt{2I_{D1}\mu_n C_{ox} \frac{W_1}{L_1}}}{\sqrt{2I_{D2}\mu_p C_{ox} \frac{W_2}{L_2}}} = -\sqrt{\frac{I_{D1}\mu_n C_{ox} \frac{W_1}{L_1}}{I_{D2}\mu_p C_{ox} \frac{W_2}{L_2}}} \end{aligned} \right\}. \quad (10)$$

and taking into account that $I_{D1}=I_{D2}=I_D$, it can obtain:

$$a_v \cong -\sqrt{\frac{\mu_n C_{ox} \frac{W_1}{L_1}}{\mu_p C_{ox} \frac{W_2}{L_2}}}. \quad (11)$$

Another advantage of this topology can be deducted from last relation: voltage gain can be set by tuning the physical dimension of the transistors and it is independent of voltage supply and bias current.

D. Common-Source Amplifier with Diode – Connected PMOS Load

The last topology implemented on educational board is common-source with combined load in order to improve the voltage gain. For this topology the load has two elements: one PMOS diode (M2) connected in parallel with a current source, as is presented in Fig 4.

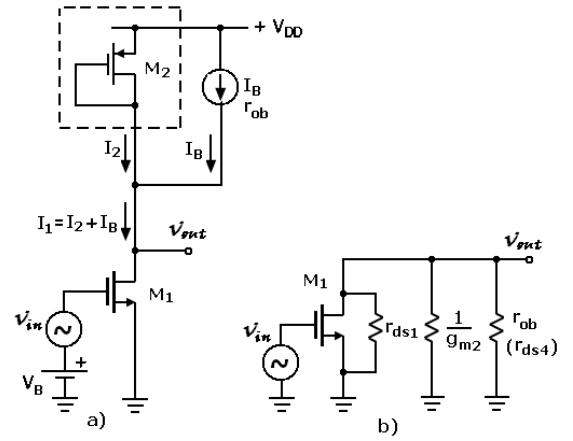


Figure 4. CS amplifier with combined load

In order to get the voltage gain for combined load CS stage it can be started with relation (10) and replace the currents I_{D1} and I_{D2} with valued imposed by electric diagram from Fig 4.

$$a_v \cong -\sqrt{\frac{I_{D1}\mu_n C_{ox} \frac{W_1}{L_1}}{I_{D2}\mu_p C_{ox} \frac{W_2}{L_2}}} = -\sqrt{\frac{(I_2 + I_B)\mu_n C_{ox} \frac{W_1}{L_1}}{I_2\mu_p C_{ox} \frac{W_2}{L_2}}}. \quad (12)$$

$$a_v \cong -\sqrt{\frac{I_2 + I_B}{I_2}} \sqrt{\frac{\mu_n C_{ox} \frac{W_1}{L_1}}{\mu_p C_{ox} \frac{W_2}{L_2}}}$$

$$a_v \cong -\sqrt{\frac{I_2 + I_B}{I_2}} \cdot a_{v_PMOS_LOAD}.$$

Relation (12) highlights that introducing current generator I_B increases the voltage gain and keeps the advantages of previous topology.

III. EDUCATIONAL BOARD PRESENTATION

The educational board presented in this section was equipped with all necessary resources in order to study all typical common-source topologies presented in previous section.

All MOSFET transistors used in this board are taken from low cost integrated circuits type CD4007 or similar [8].

The main functional blocks of educational board can be seen in Figure 5: active element; internal load; external load (signal load); input signal generator and biasing circuit for active element.

The active element used in all CS stage topologies is M1A which is taken from one CD4007 integrated circuit. For educational purposes, the channel width of active element can be doubled by closing the switch SW2.

Different type of internal load can be selected using different combinations on switches SW3, SW4 and SW5. For instance, in case of current source load, switch SW3 must be ON and the other two must be OFF. Internal current generator load is implemented with current mirror, M3&M4, which allows us to modify the value of the reference current, via selector KA.

In a similar way, passive internal load can be selected with SW5 in position ON and value of the load can be chose with selector KC. External type of load can be selected using KD. Using potentiometer P2 we can bias the active element, according with the value of I_D .

Taking into account the educational role, the board has four measuring points in order to get access to

measure different voltages or in order to use oscilloscope to display input/output signals.

This board can be used in a series of lab experiments such as:

- determination of MOSFET quadratic model parameters [9];
- studying the effect of physical dimension of the transistor over the voltage gain and over the overdrive voltage;
- studying PMOS current mirrors;
- studying common-source NMOS amplifier with different types of internal loads: resistive load, current source load, PMOS diode load, combined load (PMOS diode connected in parallel with current source);
- studying the effect of the different types of external load over the voltage gain and over the output signal waveform;

Considering all above facilities of this board which can be seen in Figure 6, I hope it will be a very useful tool in lab experiments for vocational training.

IV. EDUCATIONAL EXPERIMENTS SETUP

All transistors used in educational board are taken from low cost CD4007 integrated circuits which are mainly designed for use in logic circuits; therefore no data are available regarding the main parameters of the transistors. Even worse is that we can find big difference between circuits made by various manufacturers. From these reasons, the first experiments with this board must be targeted to more accurate determination of the main parameters of the MOSFET transistors.

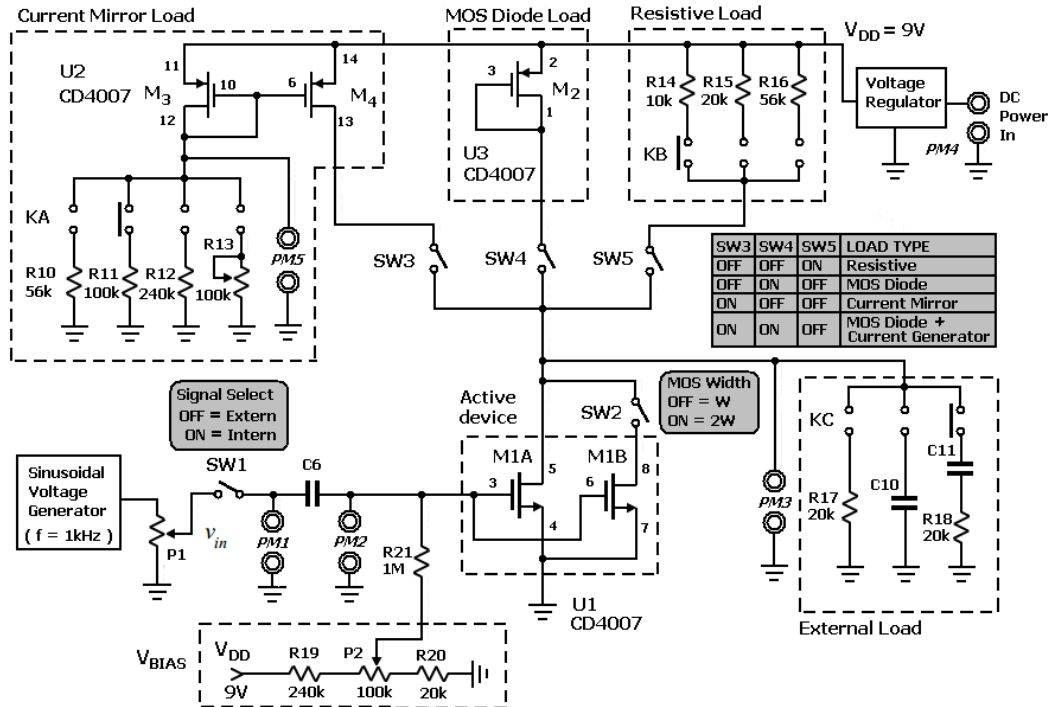


Figure 5. Block diagram of the educational board

In order to determinate the numerical values of the main parameters for NMOS transistor two measurements are needed over the gate-source voltage (V_{GS}), at two different value of drain current I_D . First V_{GS} determination (denoted V_{GS1}) is made at a current drain $I_{D1}=100\mu A$ and the second determination (denoted V_{GS2}) is made at a current drain $I_{D2} = 4I_{D1} = 400\mu A$.

For these measurements, the correct state of all switches board is OFF except SW5 which is ON. Selector KB must be in the first position in order to select $R_{14}=10k\Omega$ as a load resistor for tested transistor M1A. The value of drain current it will be tuned from potentiometer P2 until it reach the desired value, which is determined indirectly using Ohm's law.

From these measurements it can be calculate the numerical value of the threshold voltage (V_{TN}):

$$\left. \begin{aligned} I_{D1} &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{TN})^2 \\ 4I_{D1} &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{TN})^2 \end{aligned} \right\} \Rightarrow$$

$$V_{TN} = 2V_{GS1} - V_{GS2} \quad (13)$$

and then the numerical value of transconductance (g_m):

$$\left. \begin{aligned} g_{m1} &= \frac{2I_{D1}}{V_{GS1} - V_{TN}} \\ V_{TN} &= 2V_{GS1} - V_{GS2} \end{aligned} \right\} \Rightarrow$$

$$g_{m1} = \frac{2I_{D1}}{V_{GS2} - V_{GS1}} \quad (14)$$

and finally the numerical value for (K_N):

$$\left. \begin{aligned} I_{D1} &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{TN})^2 \\ I_{D1} &= \frac{1}{2} K_N (V_{GS1} - V_{TN})^2 \\ V_{TN} &= 2V_{GS1} - V_{GS2} \end{aligned} \right\} \Rightarrow$$

$$K_N = \frac{2I_{D1}}{(V_{GS2} - V_{GS1})^2} \quad (15)$$

The final step in NMOS parameters determination is validation for a third set of measurement (V_{GS3} , $I_{D3}=200\mu A$). More precisely, if the numerical values of V_{TN} and K_N are accurately determined from the first two sets of data, these value will be checked on the third sets of data (V_{GS3} , $I_{D3}=200\mu A$). If the validation step is not passed it will be necessary to remake all measurements using a better digital multimeter. Also, an increased attention should be given in numerical computing where it is necessary to use three or even four decimal places.

After determination the correct values of the NMOS transistor parameters, the same should be done for PMOS in order to determine V_{TP} and K_P . In this phase it will use only the current mirror M3&M4 and a slightly different method using also two measurements: V_{D1} - voltage from point PM5 when $R_{10}=56k\Omega$ are selected via KA; V_{D2} - voltage from point PM5 when $R_{12}=240k\Omega$ are selected via KA.

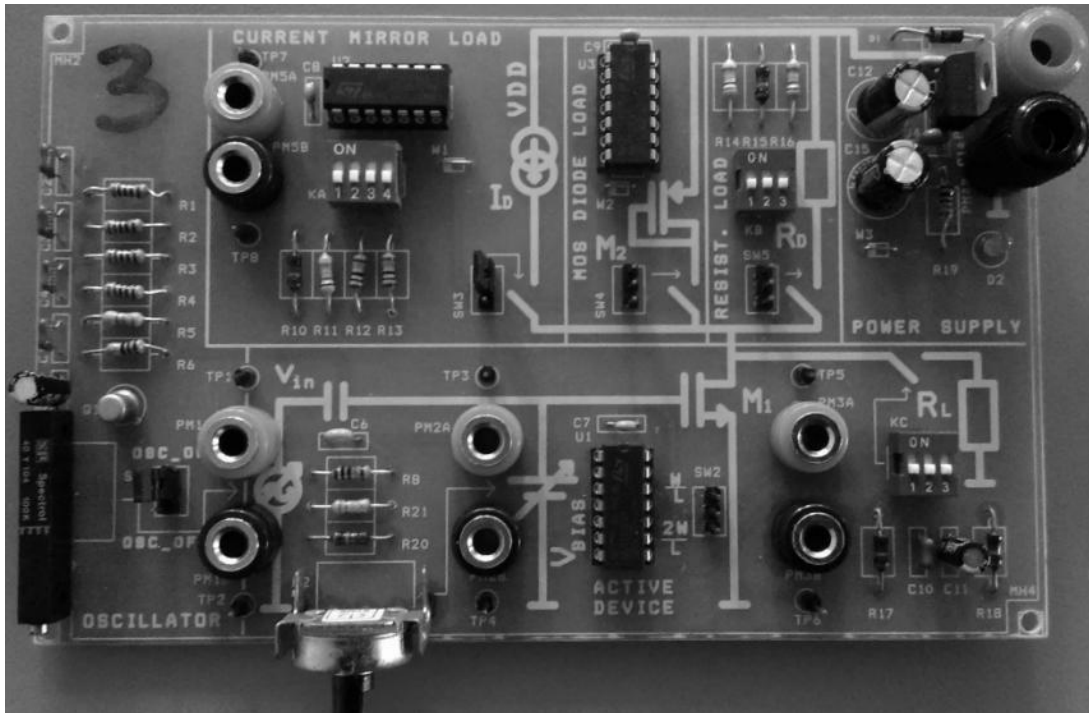


Figure 6. Practical realization of the educational board

Based on these two measurements it can be compute the numerical value of V_{TP} and K_P using the next relations:

$$\begin{cases} V_{SG1} = V_{DD} - V_{D1} \\ V_{SG2} = V_{DD} - V_{D2} \end{cases} \Rightarrow \begin{cases} I_{D1} = \frac{V_{D1}}{R_{10}} \\ I_{D2} = \frac{V_{D2}}{R_{11}} \end{cases}.$$

$$\begin{aligned} I_{D1} &= \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS1} - V_{TP})^2 \\ I_{D2} &= \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS2} - V_{TP})^2 \end{aligned} \Rightarrow \frac{I_{D2}}{I_{D1}} = \frac{(V_{GS2} - V_{TP})^2}{(V_{GS1} - V_{TP})^2}$$

$$V_{TP} = \frac{V_{GS1} \sqrt{\frac{I_{D2}}{I_{D1}}} - V_{GS2}}{\sqrt{\frac{I_{D2}}{I_{D1}}} - 1}. \quad (16)$$

$$\begin{cases} \beta_P = \frac{2I_{D1}}{(V_{GS1} - V_{TP})^2} \\ g_{m1} = \frac{2I_{D1}}{V_{GS1} - V_{TP}} \end{cases}. \quad (17)$$

Numerical value obtained with relations (16) and (17) must be verified on the third configuration obtained when $R_{11}=100k\Omega$ are selected via KA.

Experimentally determined parameters remain unchanged for the rest of the experiments as long as integrated circuits are not replaced.

Another group of optional experiments can be made for studying current mirror implemented with PMOS transistors.

The last group of experiments is more complex and more important from educational point of view; students can understand the advantage and disadvantage of different type of load used in common-source amplifiers. For each type of amplifier, correct set-up of the board can be seen in figure 5. Also students can see how voltage gain depends on a series of parameters such as: drain current, physical dimension of transistor, value of resistive load and, most important, how depend on internal load type.

V. CONCLUSION

In this paper it was presented one educational electronic board, designed by author, which can be used in vocational training, in electronic field, more specific in lab experiments regarding common-source MOSFET amplifiers with different types of loads, passive or active. Also it can be used in experiments such as: determination of MOSFET quadratic model parameters; studying PMOS current mirrors; studying the effect of physical dimension of the transistor over the voltage gain and over the overdrive voltage.

REFERENCES

- [1] European Centre for the Development of Vocational Training, "The benefits of vocational education and training, Research", Paper No10, Luxembourg: Publications Office of the European Union, 2011.
- [2] EU Documents, "Supporting vocational education and training in Europe: the Bruges Communiqué", ISBN 978-92-79-19899-1, 2011.
- [3] ProjectX, "Guidelines for making ProjectX", Lifelong Learning Programm "One teacher and one student working with ProjectX", project code 2013-1-ES1-LEO01-66485, acronym "One2one", <http://projectxone2one.eu>.
- [4] Beloiu, R., Bostan, I., Iorgulescu, I., "Internationalization of Educational Programs Through European Projects", Procedia - Social and Behavioral Sciences, vol. 180, 5 May 2015, pp. 1007-1013
- [5] Sedra, A., Smith, K.C., "Microelectronic Circuits", Oxford University Press, ISBN 9780199339143, 2015.
- [6] Allen, P., Holberg, D., "CMOS Analog Circuit Design", Oxford University Press, ISBN 9780199937424, 2012.
- [7] Razavi, B., "Design of Analog CMOS Integrated Circuits", McGraw Hill, Int. Ed, 2001.
- [8] Texas Instruments, "CD4007 Data Sheet", <http://www.ti.com/lit/ds/symlink/cd4007ub.pdf>
- [9] Zeghbroeck, B.V., "Principles of Semiconductors Devices", http://ecee.colorado.edu/~bart/book/book/chapter7/ch7_3.htm#7_3_2