Virtual Simulation and Comparison of Sine Pulse Width and Sine Duty-Cycle Modulation Drivers for Single Phase Power Inverters

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Abstract – This paper presents a comparative study of SPWM (sine pulse width modulation) and SDCM (sine duty-cycle modulation) power inverters. A unified virtual workbench is built in Multisim framework, and used for fast simulation and rapid monitoring of results. From upstream to downstream, this workbench consists of: optional SDCM and SPWM divers; a single-phase bridge power inverter, a 50 Hz filter and a load. The retained comparative criteria, rely on building hardware components, operating properties and the performance of the AC voltage delivered to the load in each case. As findings emerging from well tested prototyping systems, the SDCM-based inverter offers in most cases, smarter operating properties and better overall performance, compared to those provided by the SPWM-based inverter. Hence, the extended versions of SDCM for three-phase inverters, might become an emerging research area of control systems in power electronics.

Keywords-SDCM; SPWM; drivers, workbench; simulation; inverters.

I. INTRODUCTION

The PWM is the most popular building technique of drivers for power electronic converters [1-2]. The extended version of PWM, e.g., SPWM and SVPWM, widely used today in other to meet the operating requirements of DC-AC power converters [3-5]. In addition, the digital version of PWM, SPWM, SVPWM modules are embedded commonly into most microcontrollers, as easy-to-use digital drivers and DAC (digital-to- analog) resources [6].

In the literature, numerous comparative studies encountered on PWM techniques have been conducted within the same class of modulation policies, e.g., PWM SPWM, SPWM and SVPWM [3-5]. According to our best knowledge, comparative studies of the class of PWM drivers to other classes of drivers, are rarely encountered in the industrial electronics literature.

On the other hand, many works have been reported in the literature on DCM technique and its relevant applications including DCM drivers [7-9]. Even though in several papers, a few advantages of DCM compared to PWM have been outlined, there is a lack of deep and extended comparative studies between the two. Hence, the main aim of this paper is to conduct a deep comparative study of SDCM and SPWM drivers Jean Mbihi Research Laboratory of CSEA, ENSET University of Douala, Cameroon mbihidr@yahoo.fr

for single phase powers, using a mix of analytical reasoning and simulation of prototyping systems.

For the sake of easy understanding of this paper, let us recall the principles of basic DCM and PWM drivers for power electronic converters.





The principles of DCM and PWM drivers are recalled in Figure 1. Figure 1a shows that the DCM relies on a feedback loop structure, an embedded clock, and a modulated wave $x_m(x, t)$ with modulation frequency $f_m(x) = 1/T_m(x)$, which evolves according to a given time varying profile, dictated by the modulating x. In Figure 1b, it is worth noting that the PWM relies on an open loop multistage architecture, due to the need of a triangular clock. In this case, the

modulation frequency is constant and the sine input x is encapsulated in the pulse width duration of $x_m(x, t)$.





Unfortunately, as it will be outlined later in this paper, these apparent facts might be thought of as the main sources of numerous weaknesses of DCM techniques.

The next sections of this paper are organized as follows: In section II, the research methodology and tools for the design of a virtual workbench for SDCM-based and SPWM-Based power inverters, are presented. Followed in Section III by the presentation the prototyping virtual workbench to used for capturing a sample of relevant results. Then the comparative study of SDCM-based and PWM-based inverters are outlined in section IV. Finally, the conclusion of the paper is provided in Section V.

II. RESEARCH METHODOLOGY AND TOOLS

A. Unified Virtual Workbench for SDCM-based and SPWM-based Single Phase Power Inverters

Figure 2 shows a unified Multisim workbench of SDCM and SPWM of single-phase power inverters. The sub-diagram representation of some parts is preferable for the sake of better visualization clarity.

The proposed virtual workbench consists of main parts numbered from 1 to 9 as follows:

- (1) DCM circuit (see Figure 3).
- (2) PWM circuit (see figure 4)
- (3) DCM/PWM switch in figure 2.
- (4) SX_driver where X stands for DCM or PWM (see figure 5)
- (5) $\pm Vcc = \pm 9$ V power supply source
- (6) Single phase bridge power inverter (figure 6)

- (7) LCL filter in figure 2, where L=L1 = L2 without loss of generality.
- (8) Resistive load with R0 as default value in figure 2.
- (9) Virtual instruments in figure 2, including XSC1 and XSC2 oscilloscopes and a XFG sine generator.









Figure 6. Single phase bridge inverter (Part No 4)



B. Operational Criteria of The Virtual Workbench

Since the workbench should be used as virtual experimentation tool, for capturing the behavior of different types of electronic drivers, i.e., SDCM and SPWM circuits, a number of equivalent operating conditions are required. These equivalent conditions are expressed here in terms of identical resources, including:

- a) Power supply
- b) X-driver
- c) Power inverter
- d) LCL filter
- e) Load
- f) Basic modulation frequency
- g) Virtual instruments configuration
- h) Modulating input x(t)

Following the hardware architecture of the workbench, all modules operating downstream the DCM/PWM switch S1, are identical. Hence all conditions listed above are obviously satisfied, except the last one, which is not obvious. Indeed, even though the modulation frequency $f_{dcm}(x) = 1/T_{dcm}(x)$ depend on *x* for DCM, whereas fpwm =1/T_{pwm} is constant for PWM, the identical factor between the two is the so-called basic *modulation frequency*, given by:

$$\mathbf{f}_{\rm dcm}(0) = \mathbf{f}_{\rm pwm} \tag{1}$$

this equality is satisfied if and only if components values of the DCM and PWM circuits (see figures 2 and 3), are chosen according to Equation (2).

$$\frac{1}{(2 R4 C1) Log\left(1+2\frac{R_2}{R_3}\right)} = \frac{1}{(4 R6 C2) \frac{R5}{R1}}$$
(2)

III. PROTOTYPING VIRTUAL SIMULATION WORKBENCH

Table 1 shows the nominal data of the prototyping system considered in this paper.

TABLE I.	CHACRACTERISTICS OF THE PROTOTYPING	
	VIRTUAL WORKBENCH	

Modules	Technical characteristics		
	Part name	Reference Others	
DCM	U1A	OPAM	
	R2	1 k Ω	
	R3	8.2kΩ	
	R4	29.73kΩ	
	C1	11nF	
PWM	U4A, U5A, U6A	OPAM	
	R1	10 k Ω	
	R5	9 k Ω	
	R6	3.3k Ω	
	R7	1 k Ω	
	R8	1 k Ω	
	C2	12nF	
SX_driver	U11A	TL082CD	
	U10A, U12A, U14A	40508_10V	
	U3A	40098CL_10	
	U7A, U13A	40818D_10V	
	U2A, U15A	40508D_10V	
Briedge Inverter	Е	12V	
	Q1, Q2, Q3, Q4	IRF9640	
LCL filter	L1, L2	L = L1 = L2 = 50 mH	
	С	100uF	
Load(s)	R0	100 Ω	
	Ra	100 Ω	

As an expected result, the common basic modulation frequency given by (3), computed from DCM and PWM data in Table 1, is fdcm(0) = fpwm =7 kHz. In addition, the transfer function of the AC LCL filter (with L = L1 = L2), including the nominal load R₀ is,

$$F(s) = \frac{1}{2 L C s^{2} + \frac{2 L}{R_{0}} s + 1}$$

$$= \frac{1}{10^{-5} s^{2} + 0.001s + 1}$$
(3)

The related Bode diagram plotted in Fig. 7, indicates that a 50 Hz component which is encapsulated within a switching SDCM or SDCM output wave, can be significantly amplified through the LCL filter.



IV. MAIN VIRTUAL SIMULATION RESULTS AND PERFORMANCES COMPARISON OF SDCM AND SPWM

A. Virtual Simulation Results in The Time Domain

The main virtual simulation results conducted in the time domain, using a sine modulating signal with nominal parameters Vp = 1 volts and fs = 50 Hz, consist of:

SDCM and SPWM switching logic (see figure 8). In SDCM technique (see figure 3), the switching thresholds conditions as shown in [11], could be written by the linear feedback control policy (4). Indeed, since uC1(t) depends over time on both modulating input x and switching modulated output xm(x, t). Conversely, the SPWM technique (see figure 4), is an open loop control given by (5).

$$x_{m}(x, t) = V_{cc} s_{gn}(a x_{m}(x, t) + (1 - a) x(t) - ucl(t)),$$

with, $a = \frac{R_{2}}{R_{2} + R_{3}}$ (4)

$$xm(x, t) = Vcc \ Sgn(x - uC2)$$
(5)

- SDCM and SPWM modulating range (figure 9). In figure 9a, the maximum amplitude of the modulating input for DCM is closed to 7 volts. Whereas the maximum amplitude involved in figure 9b for PWM is 1.2 volts:
- The transient analysis of SDCM and SPWM, as shown in figure 10, indicates that, the transient time is 40 ms in each case.

Figure 8. SDCM and SPWM switching logic





Figure 10. Transient time for SDCM and SPWM



B. Virtual Simulation Results in The Freqency Domain

A sample of main virtual simulation results obtained under Multisim platform, have been exported into Matlab framework for advanced numerical analysis relying on the use of Matlab digital signal processing commands, e.g.: SNR, THD, SINAD, SFDR. The exportation process was conducted according to the following sequential steps:

- a) Creation of *.scp data file from Multisim
- b) Opening and conversion of *.scp file into

*.m files using EditPad Lite tool.

- c) Importing of *.m file into MATLAB
- d) Resampling of data, with 5 kHz sampling frequency.
- e) Comparison of original data from Multisim and the resampled version for the sake of reliable analysis.

Figure 11 shows a sample of original and resampled DCM response plotted in Matlab, whereas

Figure 9. Range of modulating x(t)

the data associated with PWM is presented in Figure 12.

Figure 11. Multisim DCM data imported into Matlab and resampled version (at 5 kHz) using Matlab



Figure 12. Multisim PWM data imported into Matlab and resampled version (at 5 kHz) using Matlab



The normalized performances of DCM-based and PWM-Based AC signals delivered to the load, as computed in Matlab, are presented and compared in

Figure 13 (for SNR), figure 14 (for THD), figure 15 (for SINAD) and figure 16 (for SFDR). These performances are described in depth in the Appendix.





Figure 14. DCM-based and PWW-based THDs



Figure 15. DCM-based and PWW-based SINADs



As a relevant finding, the normalized performances of the SDCM-based power inverter, are better in most cases than those of the SPWM-based architecture.

Figure 16. DCM-based and PWW-based SFDRs



C. Summary of The comparative Study

The relevant findings arising from this comparative study are summarized in Table II. The first column deals with comparative criteria, e.g., hardware complexity, operating properties, transient time, normalized characteristics (SNR, THD, SINAD and SFDR).

Compared to SPWM driver, the great merits of SDCM driver arising from Table II, rely on both a minimum number of building components, and smart operating properties, while offering better performance in most tested cases under the prototyping system.

 TABLE II.
 COMPARISON OF SDCM-BASED AND
 SPWM-BASED

 BASED
 DRIVERS FOR POWER INVERTERS
 SPWM-BASED

Comparative criteria	Basic drivers		
	SDCM	SPWM	
Harware complexity	01 OPAM	03 OPAMs	
	03 resistors	05 resistors	
	01 capacitor	01 capacitor	
	Square clock	Triangle clock	
Operating	Feedback loop	Open loop	
properties	fm(x) depends on x	fm is constant	
	x range: 7 V	x range: 1.2 V	
Transient	20 ms	20 ms	
SNR	53.51 dB	53.72 dB	
THD	-35.72 dB	-33.72 dB	
SINAD	35.70 db	33.84 dB	
SFDR	36.18 dB	35.99 dB	

V. CONLUSION

The virtual simulation approach conducted in this paper indicates that a basic SDCM driver for power inverters, offers under the same operating conditions, better characteristics, than the SPWM drivers. As an implication, the realization of a prototyping workbench for SDCM/SPWM power inverters, might be useful for a practical comparative study between the two. In addition, it would be highly appreciable in future research works, to extend the basic SDCM structure to a SVDCM-based architecture for threephase power inverters.

APPENDIX: NORMALIZED PERFORMANCES OF SIGNAL PROCESSING SYSTEMS

Notations

Let consider an overall signal transmission system drawn in Figure 17. The involved signals $x_r(t)$, x(t), y(t) and n(t), stand for reference input, process input, process output and noise respectively.

Figure 17. Overall signal processing system



Given these signals, the following notations are relevant for the definitions of normalized performances of the related overall signal processing system:

- S: Magnitude of the fundamental harmonic (rank n =1) of y(t)
- Sr: Magnitude of xr(t), where xr(t) is a fixed sine wave in our case
- N: Magnitude of the noise, due to the overall processing error $E_{SR} = S Sr$
- Hm = Magnitude for harmonic of rank m.
- Hmax = Max (H2, H3, ...), excluding H1.
- D : Magnitude distorsion of y(t)

Expressions of SNR, THD, SINAD and SFDR

As an implication, the normalized performances used in this paper, are defined in available references [12-13], as follows:

SNR (dB) = 20 log10
$$\left(\frac{S}{N}\right)$$
 (6)

THD (dB) = 20 log10
$$\left(\frac{S}{D}\right)$$
 (7)

SINAD (dB) =
$$20 \log_{10} \left(\frac{S}{N+D} \right)$$
 (8)

SFDR (dB) =
$$20 \log_{10} \left(\frac{H_1}{H \max} \right)$$
 (9)

Relevant comments

A few relevant comments from Equations (6)-(9) could be outlined as follows:

- Each performance is defined from a ratio between two quantities of the same physical unit, e.g., Volt in the case of this paper). Thus, it is normalized (without physical unit). Although the dB unit in not indispensable, however, it is useful as a zooming scale, for better visualization of very low real original values.
- In each case of Equations (6)-(8), the greater the value of S compared to that of N (or D), the higher the quality of the overall signal processing system. In signal processing practice, the normalized admissible range is fixed within the neighborhood of a central value, e.g., 2%, 5%, etc.
- Quantities defined by Equations (6)-(8), can be automatically computed using related Matlab commands, e.g., *snr, thd, sinad* and *sfdr*, as it has been the case in this paper.
- In Equation (9), the higher *H1* compared to Hmax, the greater the resulting *SFDR*, which can be measured in the graph of the power frequency spectrum of the output, using Matlab *sfdr* command.

CONTRIBUTIONS OF AUTHORS

Leandre Nneme Nneme contributed to: a) the introduction and research methodology; b) the design of the virtual workbench for SDCM and SPWM power inverters; c) the implementation in Multisim of the prototyping workbench: d) the presentation of virtual simulation results provided in the paper; e) the preparation and implementation in the Appendix section, of additional informations requested by anonymous reviewers, on normalized performances, i.e., SNR, THD, SINAD and SFDR.

Jean Mbihi contributed to: a) the exportation of *.*scp data file* from Multisim to Matlab via EditPad Lite tool; b) The production and presentation of the frequency analysis results provided in the paper; c) the summary of comparative results provided in Table II; d) the identification of two suitable references needed by the main author, for in depth describing of normalized performances presented in this paper; e) the work supervising as corresponding author;

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