Journal of Electrical Engineering, Electronics, Control and Computer Science – JEEECCS, Volume 8, Issue 27, pages 19-26, 2022

Pulse Power Supply for Solid State RF Amplifiers: Simulation Study and Experimental Analysis

Sachin Rathi
RF systems Division
Raja Ramanna Centre for Advanced Technology
Indore, India
srathi@rrcat.gov.in

M. K. Badapanda
RF systems Division
Raja Ramanna Centre for Advanced Technology
Indore, India
mkp@rrcat.gov.in

Rajesh Arya
Laser Electronics Division
Raja Ramanna Centre for Advanced Technology
Indore, India
rajarya@rrcat.gov.in

Akhilesh Tripathi
RF systems Division
Raja Ramanna Centre for Advanced Technology
Indore, India
atripathi@rrcat.gov.in

Rinki Upadhyay
RF systems Division
Raja Ramanna Centre for Advanced Technology
Indore, India
rinki@rrcat.gov.in

Mahendra Lad
RF systems Division
Raja Ramanna Centre for Advanced Technology
Indore, India
ladm@rrcat.gov.in

Abstract – A pulse power supply consisting of 24 numbers of 50 V, 80 A pulse power modules has been developed to bias 24 solid state RF power amplifiers simultaneously, for proton accelerator. A chopper switch based scheme has been adopted for development of these pulse power modules. This paper presents the simulation study of pulse power module and parametric sweep analysis for optimizing its circuit components like circuit inductance, snubber circuit capacitance etc. along with experimental validation of simulation results. Effects of variation in crucial circuit components on output pulse performances have been presented in this paper. The pulse width and repetition frequency of output pulse are variable from 100 µs to 2 ms and from 1 Hz to 50 Hz respectively. Heat run test of pulse power supply has been carried out on dummy resistive load for 8 hours, with simultaneous operation of pulse power modules at 80 A peak current. The rise time and fall time of output voltage pulse are found to be < 15 µs and voltage droop in output pulse is observed as < 1 %.

Keywords- Accelerator power supplies, Pulse power modules, PSpice simulations, Snubber circuit, SSPA.

I. INTRODUCTION

Radio frequency (RF) system is an important subsystem of particle accelerator. RF system provides RF power to energize charged particles (e.g. electrons and ions) which keeps them moving at very high speed in the accelerator. RF power required for various particle accelerators can be generated either by Solid State RF Power Amplifiers (SSPAs) or by vacuum tube based RF amplifiers like Klystrons, Inductive Output Tubes (IOTs) etc. [1], [2]. SSPAs are normally employed for lower RF power applications while vacuum tube based RF amplifiers are employed for higher RF power applications. Large numbers of SSPAs modules are operated in parallel to reach required power level for particle accelerators [3].

The RF power required for 1 GeV, 10 mA proton accelerator is provided by several units of SSPA based 50 kW, 325 MHz pulsed RF amplifiers. One unit of 50 kW pulsed RF source contains multiple 1.5 kW, 325 MHz pulsed SSPAs. These SSPAs are being operated simultaneously to meet RF power requirement. So a pulse power supply having 24 numbers of 50 V, 80 A pulse power modules has been developed to bias 24 numbers of 1.5 kW, 325 MHz pulsed SSPAs simultaneously.

Both, DC and pulse power supply can be employed for biasing pulsed SSPA but pulse power supply offers several advantages over its DC counterpart [4]-[7]. The ratings of switchgear elements like contactor and fuse used in DC power supplies are decided by considering their continuous full load operation [8]-[10]. If a DC power supply is employed for pulsed application, input rms current drawn by power supply will be much less, so switchgear elements used in it will be ineffective to protect its semiconductor devices and other sensitive elements. Again, when RF drive pulse is applied to a pulsed SSPA biased by DC power supply, transients may appear in RF output pulse. Further, if pulsed SSPA is biased by DC power supply, it continues to draw bias current during OFF period of RF pulse, resulting in additional power loss which leads to reduced efficiency of overall RF system [11], [12]. But if pulsed SSPA is biased by pulse power supply, the efficiency of overall system improves [13]. Due to these reasons, pulse power supply is preferred over DC power supply for biasing pulsed SSPAs.

Section II presents the design and fabrication of pulse power modules used in this pulse power supply. The theoretical analysis of one number of 50 V, 80 A

pulse power module has been presented in Section III. Simulation analysis of one number of 50 V, 80 A pulse power module has been presented in Section IV. Section V presents design of heat sink for pulse power modules. Section VI contains description of FPGA based control and protection unit used in this pulse power supply. Experimental results and analysis of this pulse power supply are presented in Section VII. Conclusion drawn from this paper is presented in Section VIII.

II. SYSTEM DESCRIPTION

The 50 V, 24 x 80 A pulse power supply contains 24 numbers of 50 V, 80 A pulse power modules for biasing solid state RF power amplifiers. Individual 50 V, 80 A pulse power module has been developed based on chopper switch scheme. Under this scheme, a capacitor bank is charged with the help of a 50 V DC power supply having output regulation and voltage stability better than 0.4 %. Further, ripple amplitude is negligible in this DC source [14]. In addition, it contains input EMI/EMC filter to remove interferences from input. The energy stored in capacitor bank is then discharged with help of MOSFET switches employed in pulse power modules thereby generating output pulses. The capacitance requirement for pulse power supply is governed by following equation:

$$I = C\,(dV/dt), \qquad (1)$$

where I = total current drawn from capacitor, C = capacitance, dV = voltage droop across output of capacitor and dt = turn ON time. For 24 pulse power modules, each having peak current output of 80 A, total current for load will be 24 x 80 = 1920 A, so to achieve voltage droop = 1 % for turn ON time = 2 ms, the capacitance requirement C = 7.68 F. This capacitance is realized by connecting 390 numbers of Illinois make 100 V, 22000 µF electrolytic capacitors in parallel combination. The current rating of DC power supply used to charge capacitor bank, is calculated by equating charge lost from capacitor bank during turn ON time to charge gained from supply during turn OFF time. This results in minimum current rating of DC power supply to be 238 A. So a DC power supply of rating 50 V, 700 A has been used. Initial surge current drawn by capacitor bank is high and can damage power circuit. To facilitate slow start charging of capacitor bank, it is initially charged through a 5/6 Ω resistor which is bypassed by means of a DC contactor after 2 minutes to avoid additional ohmic losses.

The overall scheme of pulse power supply containing 24 pulse power modules is shown in Fig. 1. The output of DC source is fed to 8.58 F capacitor bank which gets charged up to 50 V in a slow start manner, at turn ON of DC power supply. Each pulse power module can supply 80 A peak current to RF amplifier with maximum ON period of 2 ms, at maximum frequency of 50 Hz. Further, to reduce inductance, litz wires have been used for load interconnection.

The schematic of individual pulse power module is shown in Fig. 2. It contains an IXYS make 100 V, 200 A IXTH200N10T MOSFET switch, a Power Integration make 2SC0108T2F1-17 gate driver circuit, a Vishay make VS60APU02 freewheeling diode and 80 A dummy resistive load. Output load current is being sensed using LEM make LA150-P hall sensor.

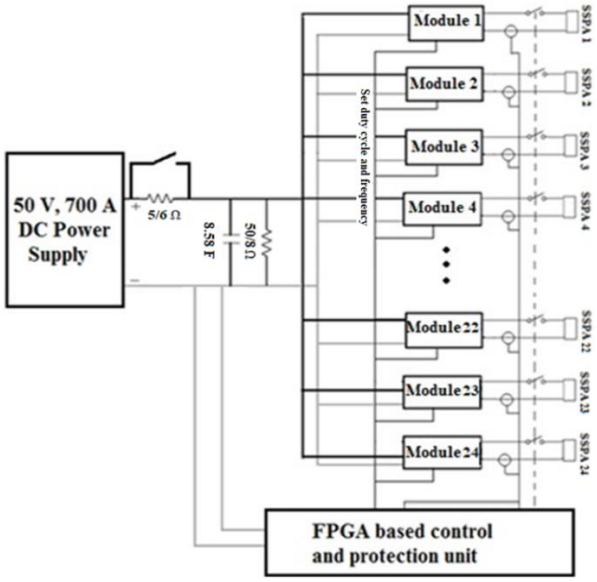

Fig. 1. Schematic of pulse power supply containing 24 pulse power modules

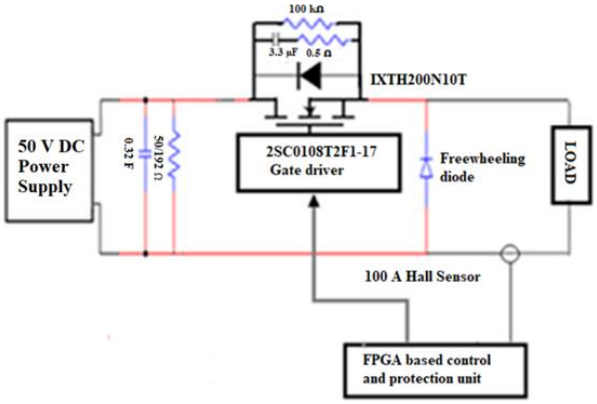

Fig. 2. Schematic of one number of pulse power module

III. THEORETICAL ANALYSIS

Various parameters of pulse power module have been analyzed by performing theoretical analysis. The initial circuit of one number of 50 V, 80 A pulse power module is shown in Fig. 3, without freewheeling diode.

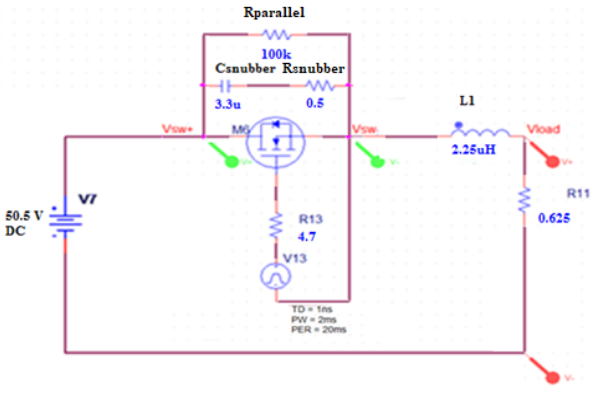

Fig. 3. Schematic of pulse power module

After optimization (described later in Section IV) snubber circuit has been added. The loop inductance of pulse power module is measured to be 2.25 µH. DC input voltage is taken as 50.5 V to account for the voltage drop across MOSFET switch in turn ON condition. By applying DC source voltage V_{DC} = 50.5 V, current flowing in circuit, at any time t (after closing the switch) is given by: I = V_{DC}/R. Output voltage across load resistance, for 80 A peak current is 80 A x 0.625 Ω = 50 V. The desired pulse width is 2 ms with time period of 20 ms. In following analysis, pulse turn OFF transition is considered at t = 0. Since before transition, capacitor was short circuited, therefore initial condition of capacitor is given by $V_C(t_{0-}) = V_C(t_{0+})$. Now simplified circuit, at t = 0 when MOSFET switch is just turned OFF, is shown in Fig. 4.

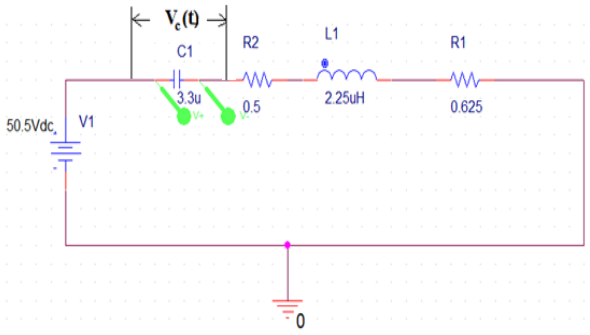

Fig. 4. Simplified circuit of pulse power module

Using circuit analysis, power circuit shown in Fig. 4 has been analyzed and voltage across MOSFET switch, which is equal to voltage across capacitor (V_C), is given by:

$$v_c(t) = e^{-\sigma t}\left[-50.5\cos(\omega_d t) + \left(\frac{80}{C\omega_d} - \frac{50.5\sigma}{\omega_d}\right)\sin(\omega_d t)\right] + 50.5 \quad (2)$$

where σ = damping ratio, ω_d = damped oscillation frequency and C = snubber capacitance for second order RLC circuit. After performing derivative analysis for maxima on (2), $V_C(t)$ is found to be maximum at t_{peak} = 6.27 µs, $V_C(t_{peak})$ = 60.65 V. So overshoot across MOSFET switch is 60.65 V in present conditions.

IV. Simulation Analysis

PSpice simulations have been carried out on pulse power module circuit to analyze it and to optimize its components values. For one pulse power module, with 1 % voltage droop for 2 ms turn ON time, capacitor requirement is given by (1). Therefore, capacitance of 0.32 F has been connected across the DC source. Gate drive applied to switch, is bipolar in nature with +15 V/-8 V for turn ON and turn OFF respectively with gate resistance of 4.7 Ω. Pulse duration is set to 2 ms. At input side a resistance of 15 mΩ has been placed in series with DC source, which represents Equivalent Series Resistance (ESR) of connecting wire from DC source to capacitor bank. The inductance in power circuit is 2.25 µH as measured in laboratory. To realize simulation circuit in which switch has its internal capacitance, a capacitance C_{DS} of 1 nF has been connected across switch. The circuit configuration is shown in Fig. 5. Corresponding voltage across MOSFET switch is shown in Fig. 6.

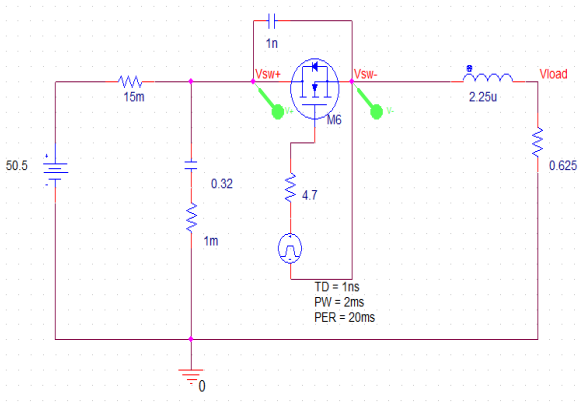

Fig. 5. Simulation circuit of a pulse power module without snubber circuit and freewheeling diode

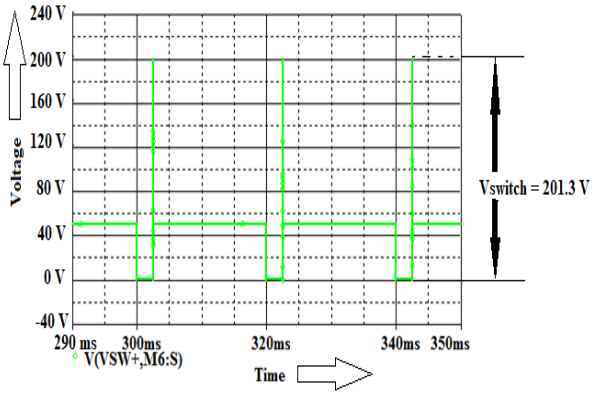

Fig. 6. Voltage across MOSFET switch without snubber circuit and freewheeling diode

As observed in Fig. 6, voltage across switch is having a peak magnitude of 201.3 V. The MOSFET switch (IXTH200N10T), used in pulse power module has drain-source breakdown voltage = 100 V, which may be detrimental for MOSFET switch [15]. In order to limit this peak voltage, R-C snubber circuit with 3.3 µF capacitance (discussed later in Section IV (B)) and 0.5 Ω series resistance has been used. This snubber circuit is connected in parallel to switch as shown in Fig. 7 and voltage waveform across MOSFET switch is shown in Fig. 8. Voltage waveform across capacitor $C_{snubber}$ is shown in Fig. 9 and voltage across load is shown in Fig. 10. As shown in Fig. 8, because of R-C snubber circuit, voltage across switch is now limited to 63.48 V. The peak voltage observed across capacitor is 60.9 V as shown in Fig. 9. This result is in close agreement with calculated overshoot from theoretical analysis, i.e., 60.65 V. Further, it can be observed in Fig. 10 that output voltage is going in negative direction with amplitude of -6.42 V. Therefore, a freewheeling diode (VS60APU02) has been connected across load as shown in Fig. 11. In this circuit, the inductance value is separated into two parts. First part, L_1 accounts for inductance between capacitor bank and pulse power module while second part, L_2 is inductance of connecting wire between pulse power module and load. To finalize values of circuit parameters, parametric sweep analysis has been performed on pulse power module. Under this, value of one component at a time is varied while rest components are kept same.

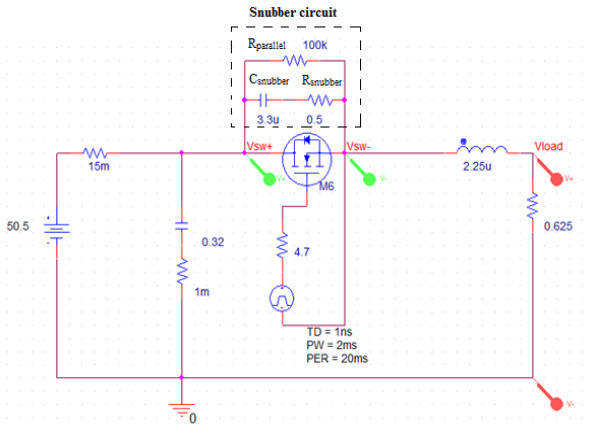

Fig. 7. Simulation circuit of a pulse power module with snubber circuit

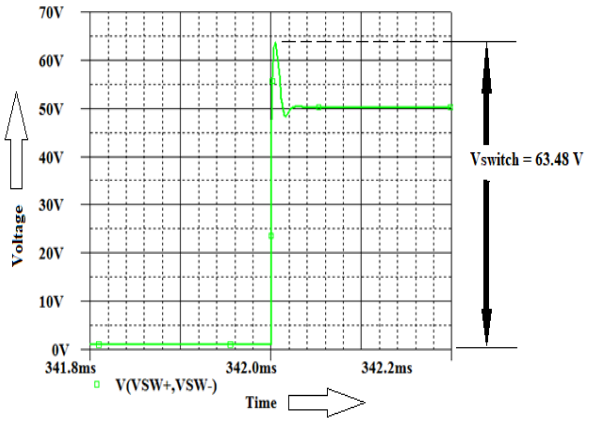

Fig. 8. Voltage across MOSFET switch with snubber circuit

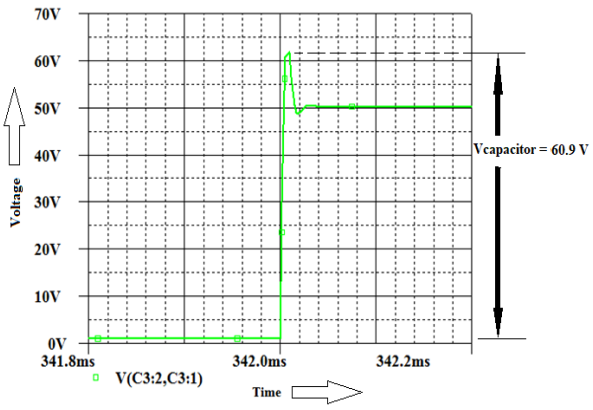

Fig. 9. Voltage across snubber capacitor $C_{snubber}$

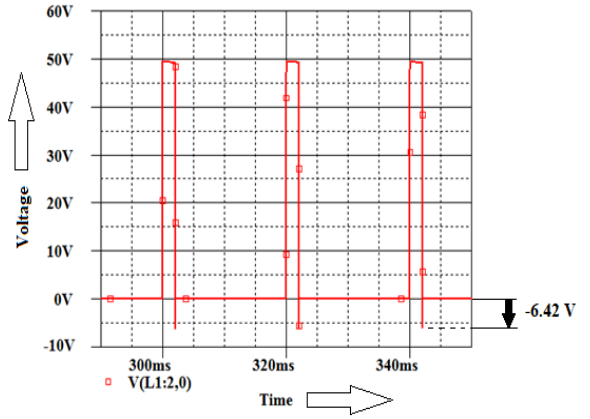

Fig. 10. Voltage across load with snubber circuit

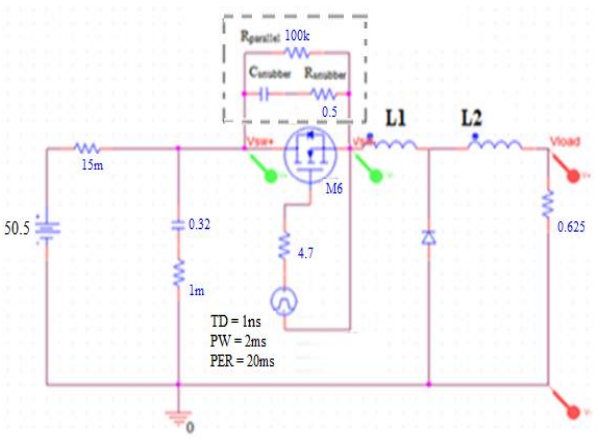

Fig. 11. Simulation circuit of a pulse power module with snubber circuit and freewheeling diode

A. Parametric sweep analysis for L_1 and L_2 :

For optimizing inductance L_1, it is varied with parameter name L_{var} from 10 nH to 500 nH in step size of 10 nH. Effect of varying inductance L_1 on rise time and fall time of output voltage pulse is shown in Table I. The simulation waveform for peak voltage across MOSFET switch as function of variable L_1 is shown in Fig. 12. It is clear from this waveform that peak voltage across MOSFET switch increases almost linearly with increase in L_1.

TABLE I. EFFECT OF L_1 ON RISE TIME AND FALL TIME OF OUTPUT VOLTAGE PULSE

L_1	Rise time t_{rise}	Fall time t_{fall}
10 nH	6.89 µs	6.59 µs
100 nH	7.19 µs	6.68 µs
250 nH	7.74 µs	6.78 µs
500 nH	8.65 µs	6.82 µs

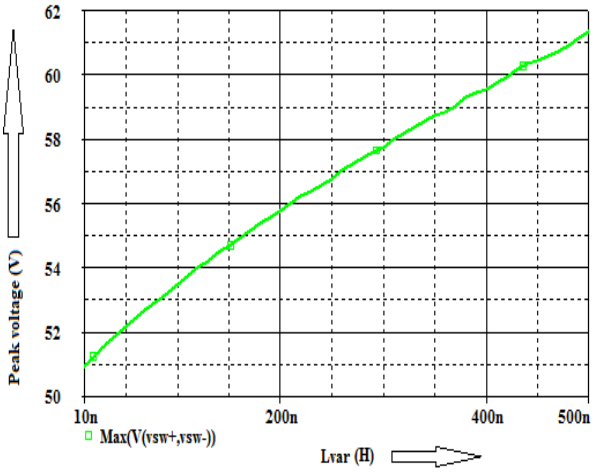

Fig. 12. Variation of peak voltage across MOSFET switch with L_1

Similarly for optimizing L_2, simulation analysis is performed, in which L_2 is varied from 1 µH to 5 µH with step size of 0.1 µH. Table II shows variation of rise time (t_{rise}) and fall time (t_{fall}) of output voltage pulse with variable inductance L_2. The simulation waveform

for peak voltage across MOSFET switch as function of variable L_2 is shown in Fig. 13. It is clear from this waveform that peak voltage across MOSFET switch increases with increase in L_2.

TABLE II. EFFECT OF L_2 ON RISE TIME AND FALL TIME OF OUTPUT VOLTAGE PULSE

L_2	Rise time t_{rise}	Fall time t_{fall}
1 µH	4.27 µs	4.27 µs
2 µH	7.74 µs	6.78 µs
3 µH	11.30 µs	10.03 µs
4 µH	14.70 µs	13.31 µs
5 µH	19.20 µs	16.66 µs

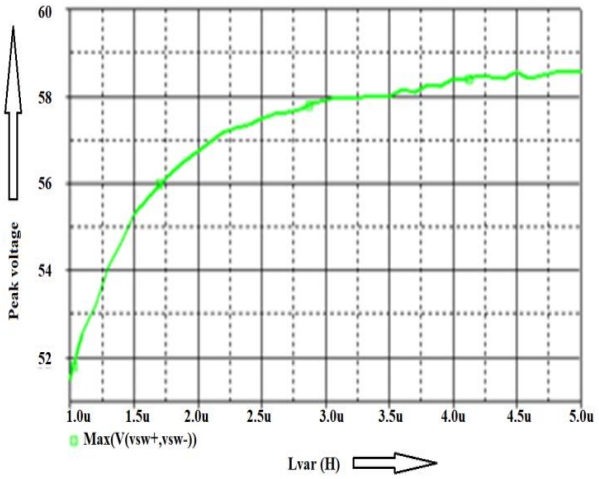

Fig. 13. Variation of peak voltage across MOSFET switch with L_2

For limiting inductance, capacitor bank is formed using copper strips. L_1 is minimized by reducing the length of wire from capacitor bank to pulse power module. L_2 is minimized by using litz wire of 4 meters length. Litz wire used in individual pulse power module has 266 strands of AWG 30 size wires and its equivalent size is AWG 6.

B. Parametric sweep analysis for $C_{snubber}$:

The snubber capacitance should be large enough to substantially reduce transients across MOSFET switch. For finding suitable value of $C_{snubber}$, it has been varied from 1 µF to 5 µF with step size of 0.1 µF. Its effect on rise time and fall time of output voltage pulse is shown in Table III. Peak voltage across switch as a function of $C_{snubber}$ is shown in Fig. 14.

TABLE III. EFFECT OF $C_{SNUBBER}$ ON RISE TIME AND FALL TIME OF OUTPUT VOLTAGE PULSE

$C_{snubber}$	Rise time t_{rise}	Fall time t_{fall}
1 µF	7.62 µs	6.63 µs
3.3 µF	7.74 µs	6.78 µs
5 µF	8.33 µs	7.18 µs

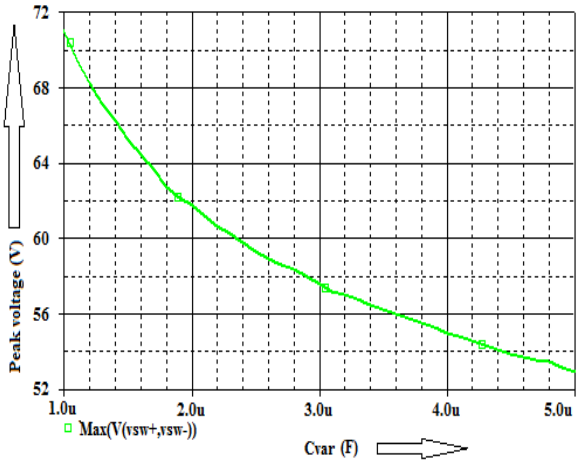

Fig. 14. Variation of peak voltage across MOSFET switch with $C_{snubber}$

As shown in Fig. 14, if $C_{snubber}$ is being varied from 1 µF to 5 µF, peak voltage across switch shows reducing trend. Thus it can be said that higher capacitance will result in reduced voltage stress on switch. However, with increasing capacitance, rise time and fall time of output pulse increase as shown in Table III. So an optimum value of 3.3 µF capacitance is chosen at which peak voltage across switch is 56.78 V.

With optimized values of L_1, L_2 and $C_{snubber}$ from parametric sweep analysis, power circuit has been simulated and corresponding voltage waveform across switch, across load, rise time and fall time of output pulse is shown in Fig. 15, 16, 17 and 18 respectively.

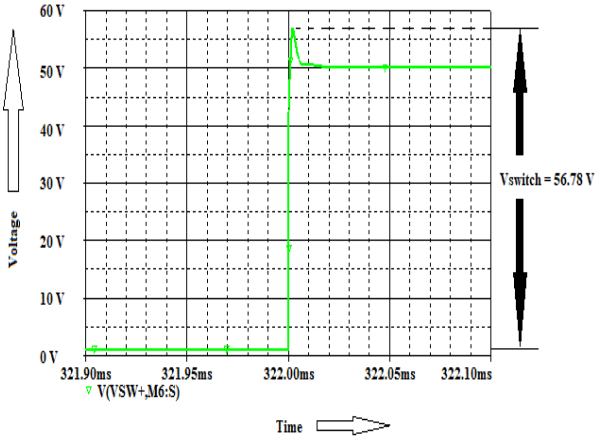

Fig. 15. Voltage waveform across MOSFET switch with snubber circuit and freewheeling diode

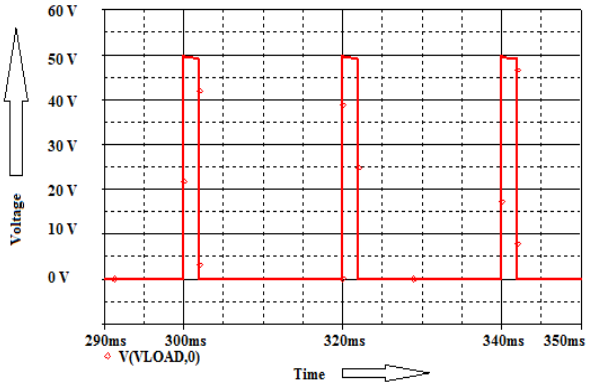

Fig. 16. Voltage waveform across load

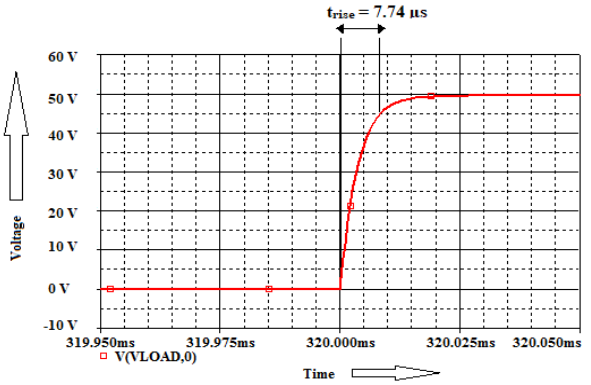

Fig. 17. Rising edge of output pulse

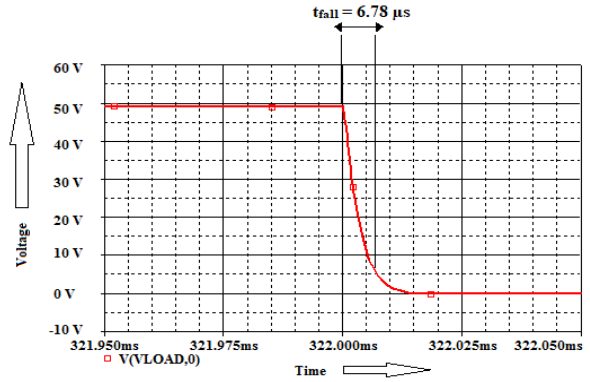

Fig. 18. Falling edge of output pulse

V. HEAT SINK SELECTION

In each pulse power module, MOSFET switches have been placed on heat sink. Dimensions of heat sink have been decided considering losses occurring in pulse power modules. These losses have been categorized into two parts namely, conduction loss and switching loss. Conduction loss occurs during turn ON of pulse is given by:

$$P_{conduction} = (I_{rms})^2 R_{ds(on)}, \quad (3)$$

where, I_{rms} is rms current through MOSFET, $R_{ds(on)}$ is ON state resistance between drain and source terminals of MOSFET and $P_{conduction}$ = conduction loss. The ON resistance of MOSFET ($R_{ds(on)}$) used in pulse power module is 11 mΩ at 100 ˚C [15]. For 10 % duty cycle and 80 A peak current, I_{rms} = 25.29 A. Putting these values in above equation, $P_{conduction}$ = 7.04 W at 100 ˚C. Due to reduced switching frequency and lower rise time and fall time of voltage across switch, switching losses are neglected. So total power dissipation P_d is given by,

$$P_d = P_{conduction} + P_{switching} = 7.04 \text{ W}.$$

For heat sink design, $\Delta\theta = P_d R_\theta$ therefore, $R_\theta = \Delta\theta / P_d$, where $\Delta\theta$ = temperature difference, R_θ = thermal resistance of heat sink. For temperature range 25 ºC to 100 ºC, $\Delta\theta$ = (100 - 25) ºC = 75 ºC and P_d = 7.04 W, R_θ is obtained as 10.65 ºC/W. Now,

$$R_\theta = R_{jc} + R_{cs} + R_{sa}.$$

Where R_{jc} = thermal resistance from junction to case, R_{cs} = thermal resistance from case to sink and R_{sa} = thermal resistance from sink to ambient. R_{jc} is taken from datasheet of the device as 0.3 ºC/W [15]. The MOSFET switch is mounted on heat sink material using a mica insulation sheet and heat sink compound, therefore R_{cs} is taken as 1 ºC/W. This gives, R_{sa} = 9.35 ºC/W. The cooling of heat sink has been done via natural convection so volumetric resistance is taken as 800 cm^3ºC/W. This gives the volume of the heat sink as volumetric resistance/ thermal resistance = 800 / 9.35 = 85.56 cm^3. Now four MOSFET switches of four pulse power modules are mounted on one heat sink so the volume of heat sink for four MOSFET switches is 4 x 85.56 = 342.24 cm^3. Hence a heat sink of dimension 25 cm (L) x 10 cm (W) x 3 cm (H) has been used for fabrication of four pulse power modules. The surface area of this heat sink is 250 cm^2.

VI. FPGA BASED CONTROL AND PROTECTION SYSTEM

An FPGA based control and protection unit has been developed to generate synchronized gate drive signals for MOSFET switches in pulse power modules [16]. Here, drive pulses required for operating these pulse power modules are generated by FPGA. The XC6SLX9TQG144C FPGA used in this Spartan-6 FPGA development board has been programmed in VHDL (Very high speed integrated circuit Hardware Description Language) programming language using Xilinx ISE 14.7 project navigator for pulse generation and external control of pulse parameters [17]. Further, the pulse width of output pulse is settable from 100 µs to 2 ms and frequency is settable from 1 Hz to 50 Hz.

VII. EXPERIMENTAL RESULTS AND ANALYSIS

The fabricated pulse power supply with 24 numbers of 50 V, 80 A pulse power modules is shown in Fig. 19. All pulse power modules have been simultaneously tested on dummy load, at 80 A peak current, with 10 % duty cycle at 50 Hz. An output voltage pulse and its rise time, fall time are shown in Fig. 20, Fig. 21 (a) and Fig. 21 (b) respectively. Fig. 22 shows voltage droop in output voltage pulse along with output current. The voltage overshoot across MOSFET switch during its turn OFF operation is shown in Fig. 23.

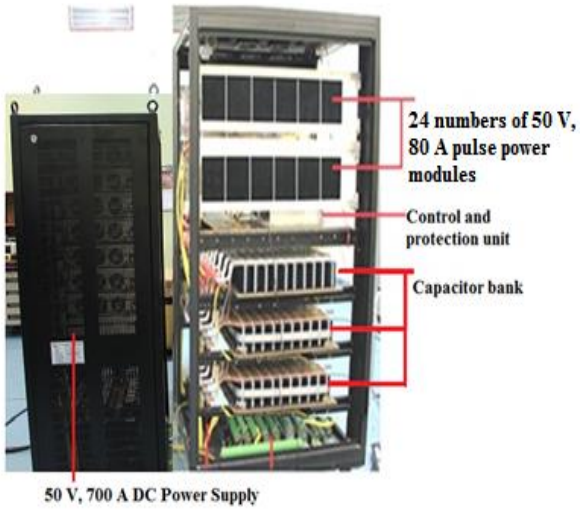

Fig. 19. Fabricated pulse power supply having 24 numbers of 50 V, 80 A pulse power modules

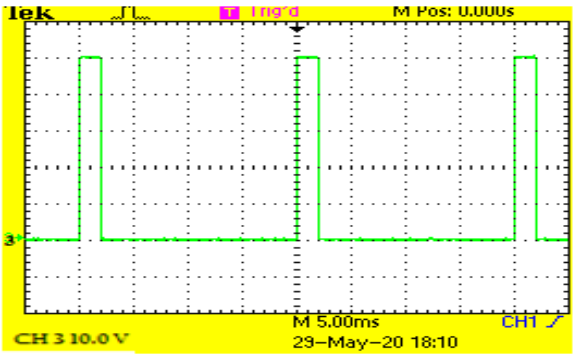

Fig. 20. Output voltage pulse of 2 ms pulse width

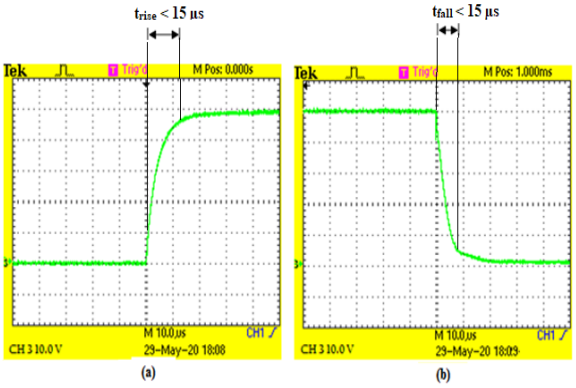

Fig. 21. (a) Rise time < 15 µs (b) Fall time < 15 µs

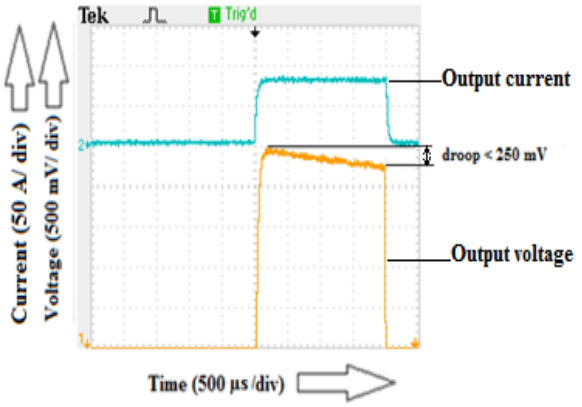

Fig. 22. Droop in output voltage pulse

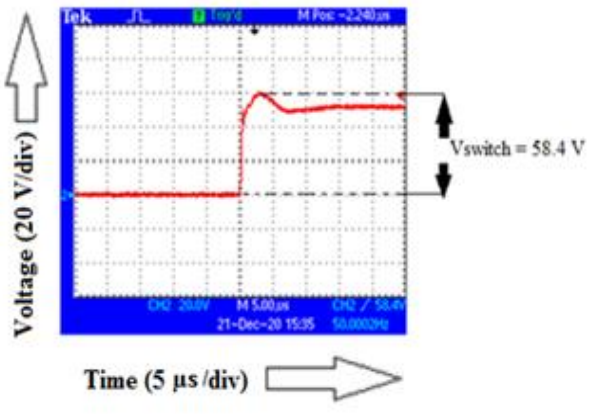

Fig. 23. Voltage across MOSFET switch during its turn OFF

Voltage across MOSFET switch has been reduced to 58.4 V by using precautions such as using litz wires for load connection, freewheeling diode, copper strips etc. Heat run test has been conducted on pulse power modules for 8 hours duration and external temperature rise of MOSFET switch during this heat run test is shown in Fig. 24. The external temperature of MOSFET switch has been recorded to be 42.8 ˚C at the end of heat run test.

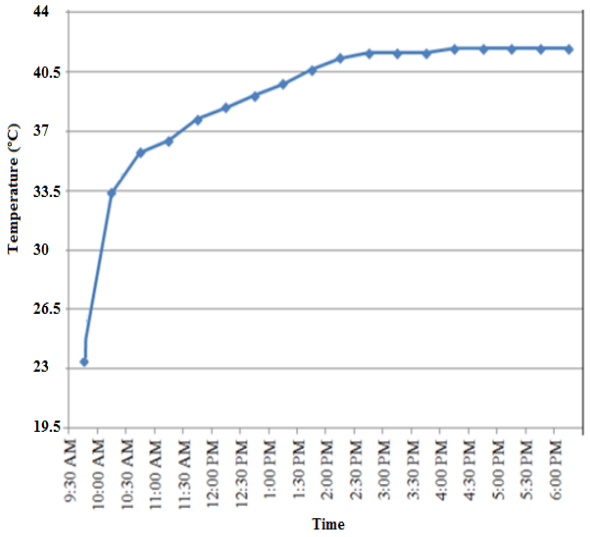

Fig. 24. External temperature of MOSFET switch during heat run test

CONCLUSION

The pulse power supply has been realized by charging a capacitor bank from a 50 V, 700 A DC power supply and discharging its stored energy with help of MOSFET switches employed in pulse power modules. This pulse power supply can bias 24 numbers of pulsed solid state RF amplifiers simultaneously with maximum ON time 2 ms at 50 Hz. Adequate steps have been taken to reduce circuit inductance by using litz wires and minimizing length of interconnecting wire in power modules. The theoretical analysis of power circuit of 50 V, 80 A pulse power module has been carried out. The simulation analysis of power module along with parametric sweep analysis of crucial circuit components has been carried out for optimizing circuit components to achieve desired output pulse performance. An FPGA based control and protection unit has been developed to generate synchronized gate drive signals to MOSFET switches. All pulse power modules have been tested simultaneously on 80 A dummy resistive load. The rise time and fall time of output voltage pulse are less than 15 µs, pulse droop is less than 0.5 % and voltage overshoot across MOSFET switch during its turn OFF operation is less than 58.4 V. Continuous heat run test for 8 hours has been carried out on developed power supply with simultaneous operation of 24 numbers of 50 V, 80 A pulse power modules, during which maximum external temperature of MOSFET switch was recorded at 42.8 ˚C.

REFERENCES

[1] R.G. Carter, “RF power generation,” CERN Yellow Report CERN-2011-007, pp.173-20, 2011.

[2] R.G. Carter, “Microwave and RF Vacuum Electronic Power Sources,” Cambridge University Press, 2018.

[3] A. Jain, D.K. Sharma, A.K. Gupta, P.R. Hannurkar, “High power solid state RF amplifier for proton accelerator,” Review of Scientific Instruments, Vol. 79, 2008.

[4] H. S. Song, S. H. Lee, M. Ghergherehchi, H. S. Kim, J. C. Lee, S. Y. Oh et. al., "Modular 20 kW, 83.2-MHz Solid-State RF Amplifier for a 10-MeV Cyclotron," IEEE Transactions on Nuclear Science, vol. 66, no. 8, pp. 1924-1930. doi: 10.1109/TNS.2019.2925407, 2019.

[5] A. Jain, P.R. Hannurkar, D.K. Sharma, A.K. Gupta, A. K. Tiwari, M. Lad, R. Kumar, M. K. Badapanda, P. D. Gupta, "Modular 20 kW solid state RF amplifier for Indus-2 Synchrotron radiation source," Nuclear Instruments and Methods in Physics Research A, vol. 676, p. 74-83, 2012.

[6] M. Gaspar and T. Garvey, "A Compact 500 MHz 65 kW Solid-State Power Amplifier for Accelerator Applications," IEEE Transactions on Nuclear Science, vol. 63, no. 2, pp. 699-706, 2016.

[7] R.K. Deo, M.K. Jain, and M. Lad, "Development of 5 kW, 1 MHz Solid State RF Pulsed Power Amplifier Using Parallel Configuration of Four LDMOS Transistor at Device and Operated in Single Ended Mode," International Journal of Advances in Microwave Technology (IJAMT), vol. 4, no. 4, pp. 208-212, 2019.

[8] A. Kumrawat, K. Saichand and V. John, "Design of AC-DC control power supply with wide input voltage variation," Proceedings of IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia), Bangalore, India, 1-6, doi: https://doi.org/10.1109 /ISGT-Asia.2013.6698779, 2013.

[9] "IEEE recommended Practice for the Application of Low-Voltage Circuit Breakers in Industrial and Commercial Power Systems," IEEE Std 3004.5-2014, v1, 2015.

[10] M. K. Badapanda, R. Upadhyay, A. Tripathi, R.K. Tyagi, M. Lad, "Modular hot swappable 50 V, 700 A DC power supply with active redundancy," Indian Particle Accelerator Conference InPAC-2015, TIFR Mumbai, 2015.

[11] R. K. Deo, G. Anghore, M.K. Jain and M. Lad, "Design and development of 3 kW pulsed solid-state RF power amplifier using two LDMOS in parallel configuration at 1 MHz," Journal of Instrumentation, 13, T12002, doi: https://doi.org/10.1088/1748-0221/13/12/t12002, 2018.

[12] L. Hoang Duc, M. Jobs, T. Lofnes, R. Ruber, J. Olsson, and D. Dancila, "Feedback compensated 10 kW solid-state pulsed power amplifier at 352 MHz for particle accelerators," Review of Scientific Instruments, vol. 90, 104707, 2019.

[13] A. Tripathi, M. K. Badapanda, R. Upadhyay, M. Lad, "Design and development of 50 V, 300 A pulse power supply for solid state RF amplifiers," Indian Particle Accelerator Conference InPAC-2015, TIFR Mumbai, 2015.

[14] R. Upadhyay, M. K. Badapanda, A. Tripathi, M. Lad, "Low voltage high current modular DC power supply for solid state RF amplifiers," Jour. of Instr., vol. 16, no. 3, pp. 1-14, 2021.

[15] IXYS corporation, "IXTH200N10T datasheet," [Online] Available:https://m.littelfuse.com/~/media/electronics/datasheets/discrete_mosfets/littelfuse_discrete_mosfets_n-channel_trench_gate_ixt_200n10t_datasheet.pdf.pdf, 2008.

[16] A. Tripathi, A. Singh, S. Rathi, R. Upadhyay, M. K. Badapanda, M. Lad, "FPGA based control and protection unit of a multichannel pulsed power supply for solid state RF amplifiers," Journal on Electrical Engineering, vol. 13, no. 4, p. 49-60, Nov. 2020.

[17] Florin-Marian Birleanu, "CHDL1: Implementing a simplified version of the Compact HDL hardware description language," Journal of Electrical Engineering, Electronics, Control and Computer Science, 2018, Vol. 4, Issue 14, pp. 17-22.